

PHK28NQ03LT

N-channel TrenchMOS logic level FET

Rev. 03 — 8 December 2009

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

1.2 Features and benefits

- Simple gate drive required due to low gate charge
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC converters
- Switched-mode power supplies

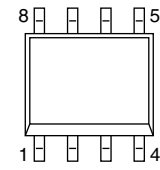
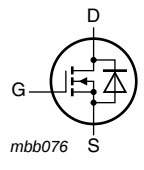
1.4 Quick reference data

Table 1. Quick reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ }^{\circ}\text{C}$; $T_j \leq 150\text{ }^{\circ}\text{C}$	-	-	30	V
I_D	drain current	$T_{sp} = 25\text{ }^{\circ}\text{C}$; $V_{GS} = 10\text{ V}$; see Figure 1 and 3	-	-	23.7	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ }^{\circ}\text{C}$; see Figure 2	-	-	6.25	W
Dynamic characteristics						
Q_{GD}	gate-drain charge	$V_{GS} = 4.5\text{ V}$; $I_D = 14\text{ A}$; $V_{DS} = 15\text{ V}$; $T_j = 25\text{ }^{\circ}\text{C}$; see Figure 11	-	11.4	-	nC
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 14\text{ A}$; $T_j = 25\text{ }^{\circ}\text{C}$; see Figure 9 and 10	-	5.5	6.5	m Ω

2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S	source	 SOT96-1 (SO8)	 mbb076
2	S	source		
3	S	source		
4	G	gate		
5	D	drain		
6	D	drain		
7	D	drain		
8	D	drain		

3. Ordering information

Table 3. Ordering information

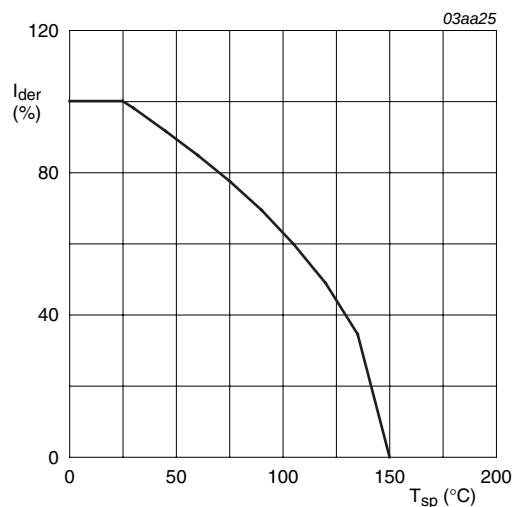
Type number	Package		Version
	Name	Description	
PHK28NQ03LT	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

4. Limiting values

Table 4. Limiting values

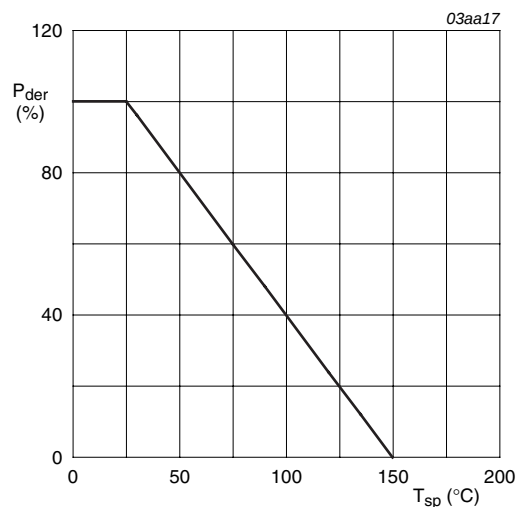
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$T_j \geq 25\text{ °C}$; $T_j \leq 150\text{ °C}$	-	30	V
V_{DGR}	drain-gate voltage	$T_j \leq 150\text{ °C}$; $T_j \geq 25\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	30	V
V_{GS}	gate-source voltage		-	20	V
I_D	limiting drain current	$T_{sp} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1	-	15	A
	drain current	$T_{sp} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; see Figure 1 and 3	-	23.7	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ °C}$; $t_p \leq 10\text{ }\mu\text{s}$; pulsed; see Figure 3	-	60	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ °C}$; see Figure 2	-	6.25	W
T_{stg}	storage temperature		-55	150	°C
T_j	junction temperature		-55	150	°C
Source-drain diode					
I_S	source current	$T_{sp} = 25\text{ °C}$	-	5.2	A
I_{SM}	peak source current	$T_{sp} = 25\text{ °C}$; $t_p \leq 10\text{ }\mu\text{s}$; pulsed	-	20.8	A



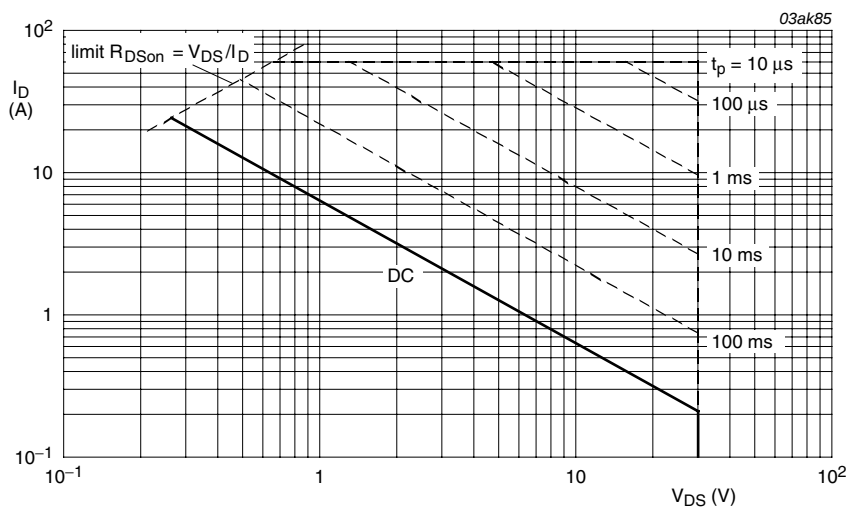
$$I_{der} = \frac{I_D}{I_{D(25^\circ\text{C})}} \times 100\%$$

Fig 1. Normalized continuous drain current as a function of solder point temperature



$$P_{der} = \frac{P_{tot}}{P_{tot(25^\circ\text{C})}} \times 100\%$$

Fig 2. Normalized total power dissipation as a function of solder point temperature



$T_{sp} = 25^\circ\text{C}$; I_{DM} is single pulse; $V_{GS} = 10\text{V}$

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	see Figure 4	-	-	20	K/W

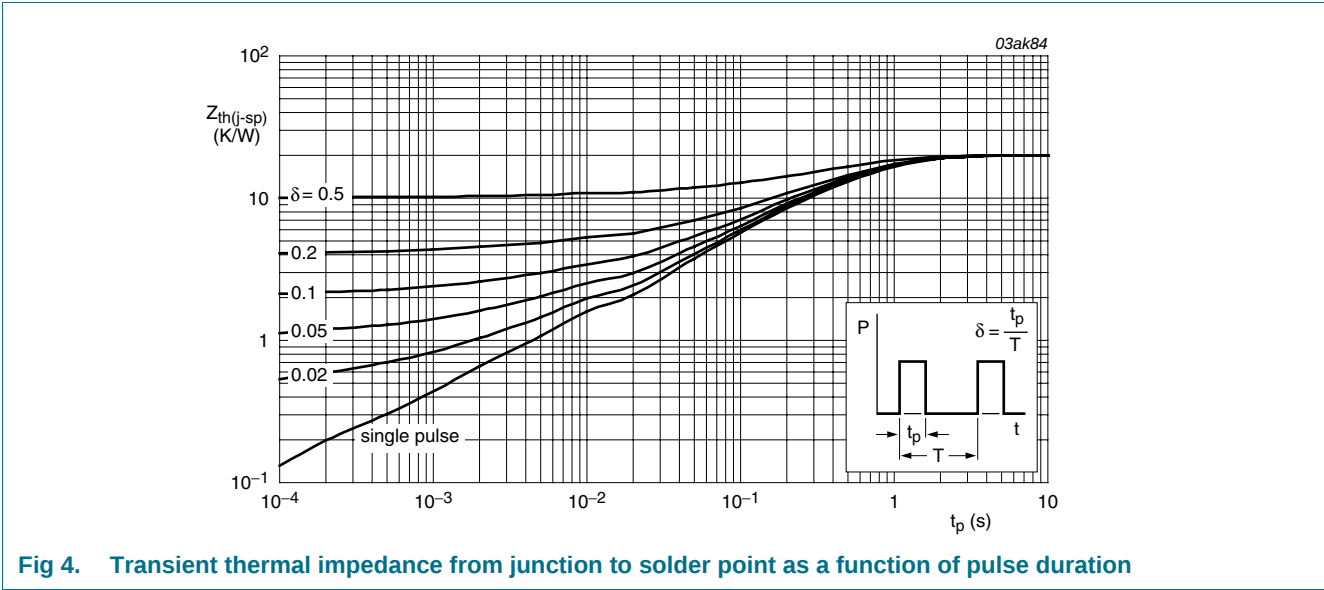


Fig 4. Transient thermal impedance from junction to solder point as a function of pulse duration

6. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V; T _j = 25 °C	30	-	-	V
		I _D = 250 μA; V _{GS} = 0 V; T _j = -55 °C	27	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 150 °C; see Figure 8	0.6	-	-	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = -55 °C; see Figure 8	-	-	2.2	V
		I _D = 1 mA; V _{DS} = V _{GS} ; T _j = 25 °C; see Figure 8	1	1.5	2	V
I _{DSS}	drain leakage current	V _{DS} = 30 V; V _{GS} = 0 V; T _j = 150 °C	-	-	500	μA
		V _{DS} = 30 V; V _{GS} = 0 V; T _j = 25 °C	-	0.05	1	μA
I _{GSS}	gate leakage current	V _{GS} = 16 V; V _{DS} = 0 V; T _j = 25 °C	-	10	100	nA
		V _{GS} = -16 V; V _{DS} = 0 V; T _j = 25 °C	-	10	100	nA
R _{DSon}	drain-source on-state resistance	V _{GS} = 4.5 V; I _D = 13 A; T _j = 150 °C; see Figure 9 and 10	-	11.2	13.1	mΩ
		V _{GS} = 10 V; I _D = 14 A; T _j = 25 °C; see Figure 9 and 10	-	5.5	6.5	mΩ
		V _{GS} = 4.5 V; I _D = 13 A; T _j = 25 °C; see Figure 9 and 10	-	6.6	7.7	mΩ
Dynamic characteristics						
Q _{G(tot)}	total gate charge	I _D = 14 A; V _{DS} = 15 V; V _{GS} = 4.5 V; T _j = 25 °C; see Figure 11	-	30.3	-	nC
Q _{GS}	gate-source charge		-	7.8	-	nC
Q _{GD}	gate-drain charge		-	11.4	-	nC
C _{iss}	input capacitance	V _{DS} = 20 V; V _{GS} = 0 V; f = 1 MHz; T _j = 25 °C; see Figure 12	-	2800	-	pF
C _{oss}	output capacitance		-	670	-	pF
C _{rss}	reverse transfer capacitance		-	320	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = 15 V; R _L = 15 Ω; V _{GS} = 10 V; R _{G(ext)} = 6 Ω; T _j = 25 °C	-	11	-	ns
t _r	rise time		-	10	-	ns
t _{d(off)}	turn-off delay time		-	80	-	ns
t _f	fall time		-	40	-	ns
Source-drain diode						
V _{SD}	source-drain voltage	I _S = 2.3 A; V _{GS} = 0 V; T _j = 25 °C; see Figure 13	-	0.72	1.2	V

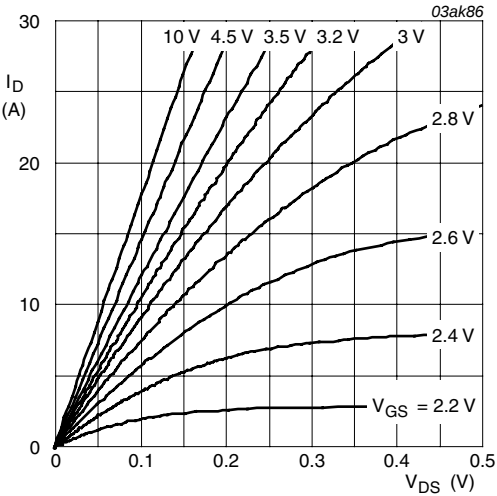


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

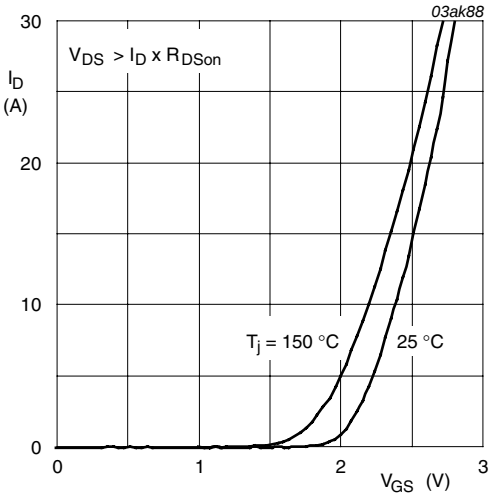


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

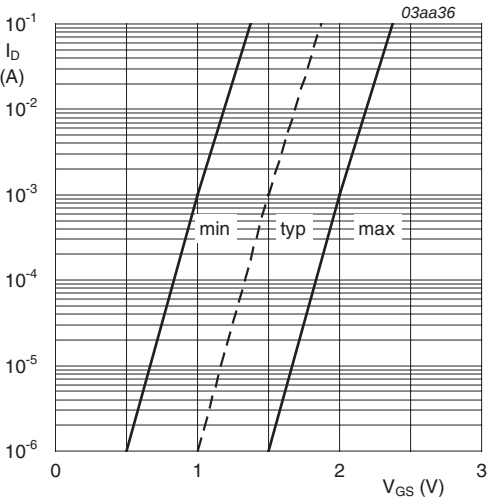


Fig 7. Sub-threshold drain current as a function of gate-source voltage

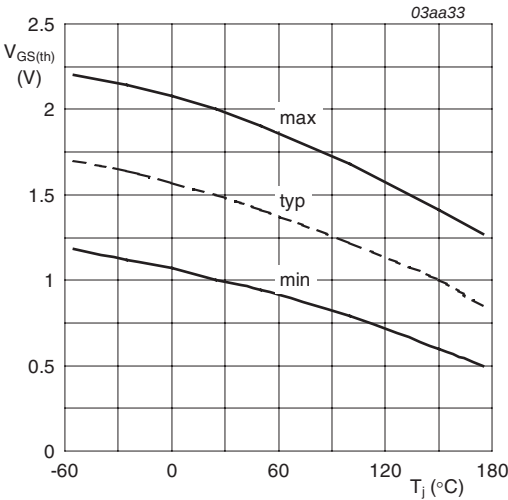
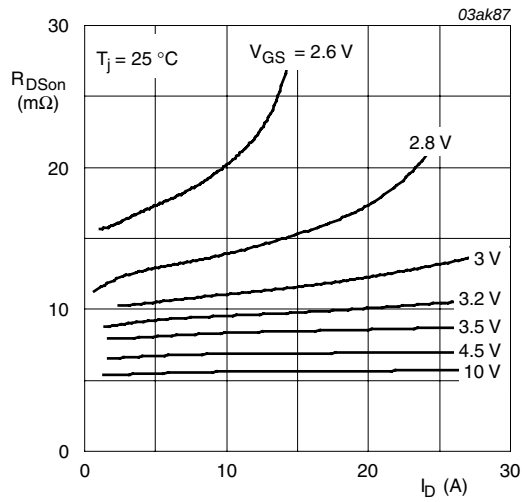
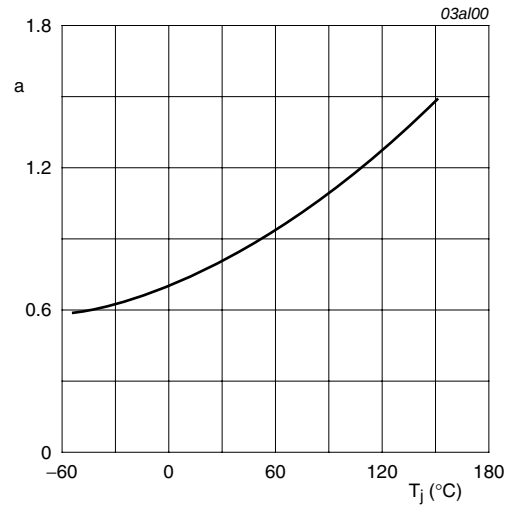


Fig 8. Gate-source threshold voltage as a function of junction temperature



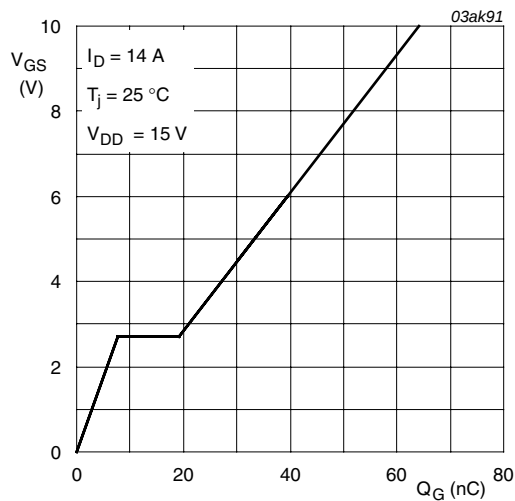
$T_j = 25^\circ\text{C}$

Fig 9. Drain-source on-state resistance as a function of drain current; typical values



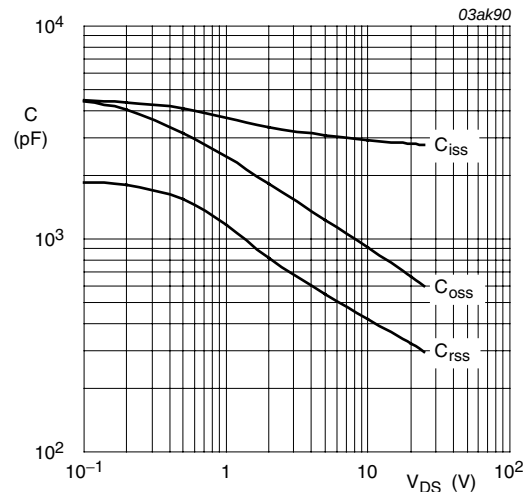
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

Fig 10. Normalized drain-source on-state resistance factor as a function of junction temperature



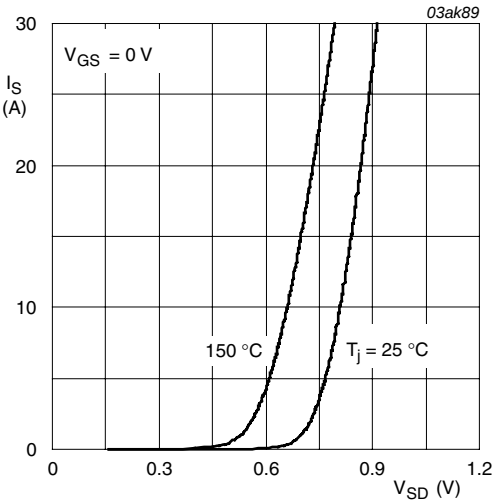
$I_D = 14\text{A}; V_{DD} = 15\text{V}$

Fig 11. Gate-source voltage as a function of gate charge; typical values



$V_{GS} = 0\text{V}; f = 1\text{MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$T_j = 25^\circ\text{C}$ and 150°C ; $V_{GS} = 0\text{ V}$

Fig 13. Source current as a function of source-drain voltage; typical values

7. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

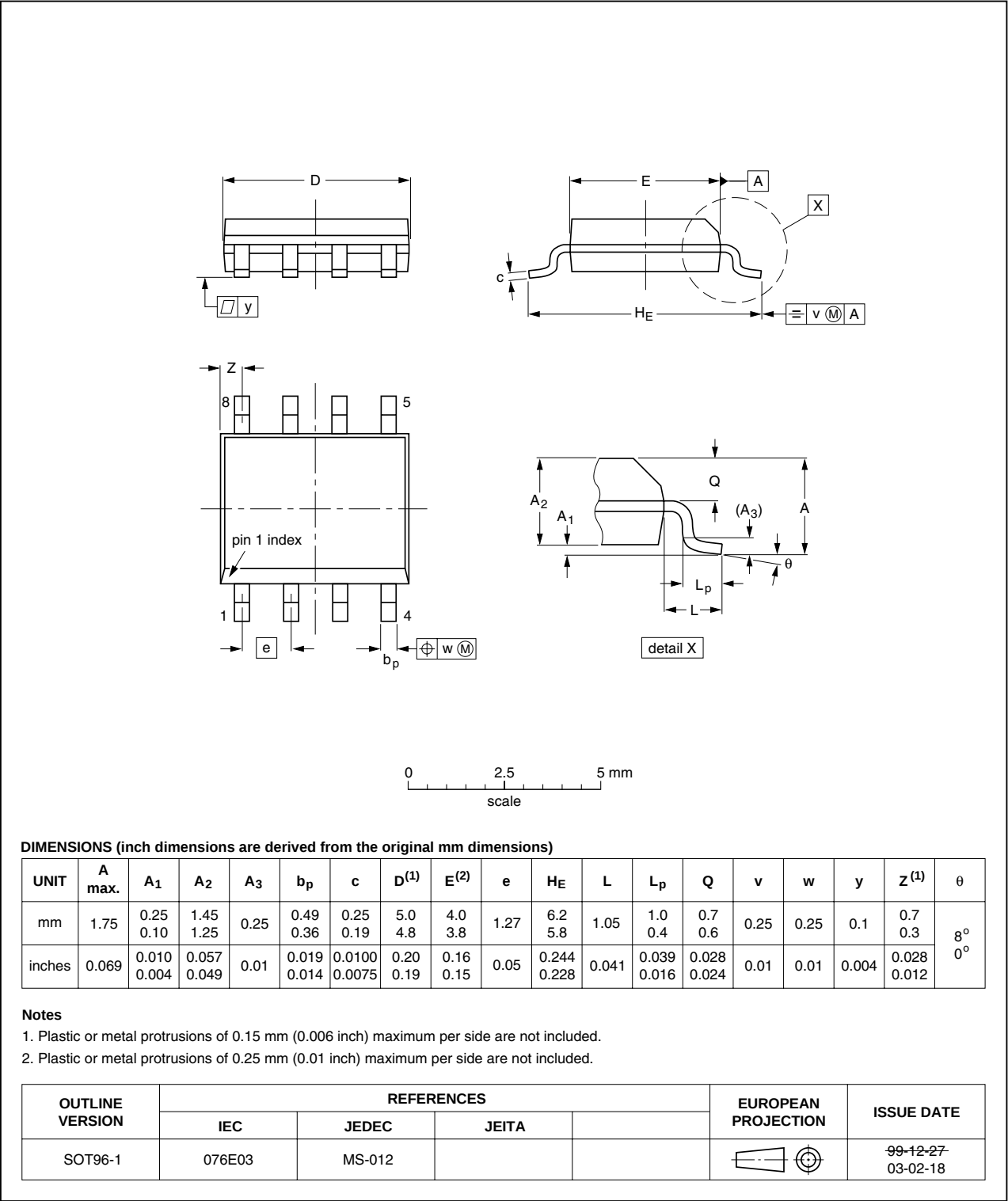


Fig 14. Package outline SOT96-1 (SO8)

8. Revision history

Table 7. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PHK28NQ03LT_3	20091208	Product data sheet	-	PHK28NQ03LT-02
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate.			
PHK28NQ03LT-02 (9397 750 11367)	20030410	Product data	-	PHK28NQ03LT-01
PHK28NQ03LT-01 (9397 750 10743)	20021212	Product data	-	-

9. Legal information

9.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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